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Improved Low Voltage High Speed FVF Based Current Comparator with Logical Efforts

Vinod Kumar, Ms. Himani Mittal, Mr. Sumit Khandelwal
M.Tech (VLSI Design), Department of ECE, JSSATE, Noida, UP (India)
Assistant Professor, Department of ECE, JSSATE, Noida, UP (India)
Assistant Professor, Department of ECE, JSSATE, Noida, UP (India)

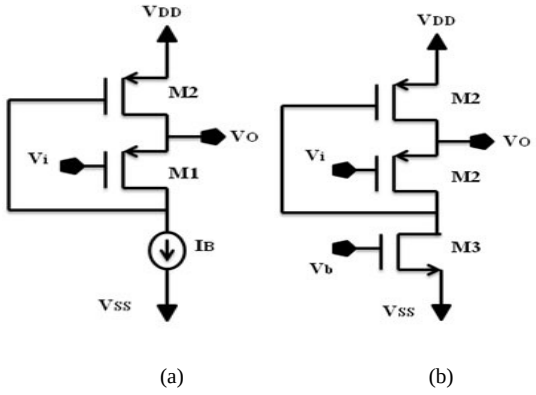
Abstract
In this paper an improved current comparator is using flipped voltage follower (FVF) to obtain the single supply voltage. This circuit has short propagation delay and occupies a small chip area. All circuits have been simulated employing Tanner EDA Tool 14.1v for 90nm CMOS technology and a comparison has been performed with its non FVF counterpart to contrast its effectiveness, simplicity, compactness and low power consumption.
Index Terms –Current Comparator, Flipped Voltage Follower, Power Consumption, Low Voltage, Propagation Delay.

I. INTRODUCTION

Current comparator is a fundamental component of current-mode circuits.In recent years, current- mode circuits have become increasingly popular among analog circuits designers. This is mainly attributed to higher speed, larger bandwidth and lower supply voltage requirement compared to its voltage mode circuit counterpart. Current Comparator is widely used as a building block for analog systems including A/D converters, Oscillators and other signal processing applications [4]. Many signal sources from temperature sensors, photo sensors generating very small current are required to be detected by low current comparators [7]. It is necessary to develop new design techniques to overcome power consumption of the digital circuitry in VLSI systems and to prevent oxide breakdown with decreasing gate-oxide thickness. Because devices scale down, the supply voltage reduces while the threshold voltage of MOSFETs downscales not as much and the short channel effects become increasingly phenomenal [1]. This factor diminishes the room for tradeoffs and hence toughens the design of a conventional source follower to meet the requirements of wide input swing and resistive load capability for the state-of-art circuits. Low voltage and low power application demands confront voltage mode IC designs, for there is less dynamic available under low power supply condition. While the circuit implemented in current mode technique occupies small area, consumes less power dissipation and achieves more dynamic range and high operation speed. Thus the current mode circuit design methodology receives increasing wide attention in the recent years [6]. It is important that comparators are high speed, but if they are to be distributed across a processing array then they must also be low power. The paper is organized as follows: The concept of FVF cell and its applications are presented in Section II. Section III describes the current comparator configurations while Section IV elaborates related works on comparator structure. The simulations and comparison results are demonstrated in Section V. Finally, in Section VI, conclusions are drawn.

II. FLIPPED VOLTAGE FOLLOWER

FVF is basically a Source Follower with shunt feedback and current/voltage biasing as can be seen from Fig. 1. Because of the shunt feedback, transistor M2 remains always in active state no matter how small power supply is given to the circuit [1]. The application of the shunt feedback extracts the whole circuit from saturation state to the active state.



(a) (b)

Fig. 1. (a) FVF using current bias (b) FVF using voltage bias [2]

Current through transistor M1 is held constant, due to current biasing. This change in output current does not

affect the input current and V_{SG1} (which is a function of input current) remains almost constant across transistorM1.This result is almost unity voltage gain or in other words output voltage follows input voltage.

Unlike the conventional voltage follower, the circuit in Fig 1(a) [1] is capable to source a large amount of current, but its sinking capability is limited by the biasing current source I_B, the large sourcing capability is due to the low impedance at the output node ($r_0=1/g_{m1}$ g_{m2} r_{01}), where g_{mi} and r_{oi} are the transconductance and output resistance respectively [1].

III. CIRCUIT STRUCTURES

This paper focuses on implementing a current comparator using a flipped voltage follower to harness the potential of FVF cell for the design of high-performance low-power/low voltage analog and mixed-signal circuits. The input stage in [1] is replaced by a FVF Source follower cell which works on 1.2V power supply.

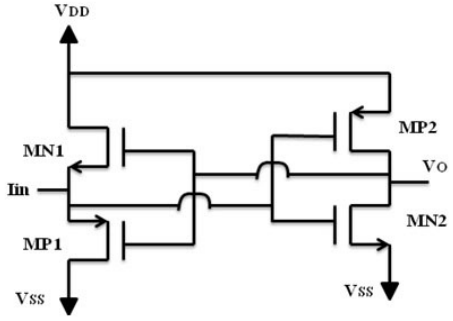


Fig. 2. Current comparator proposed by Traff

The FVF based current comparator structure has an inverter stage at the output, for amplification purpose to obtain a complete output swing [1]. In contrast, the Traff comparator gives a complete output swing when 4 inverter stages are added at the output as illustrated in Fig. 4 [1].

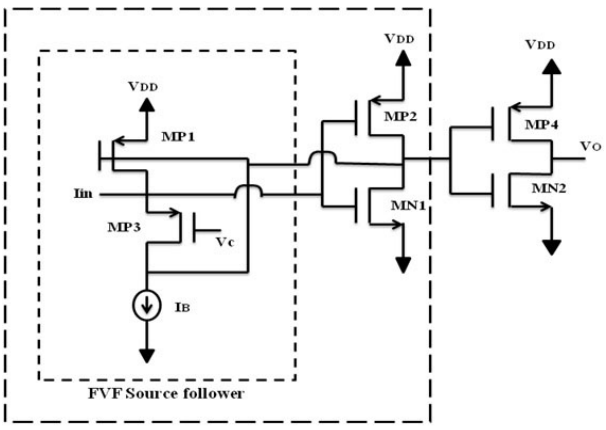


Fig. 3. FVF based Current Comparator

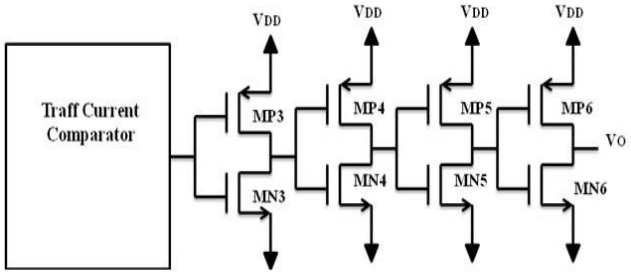


Fig. 4. Modified Traff current comparator

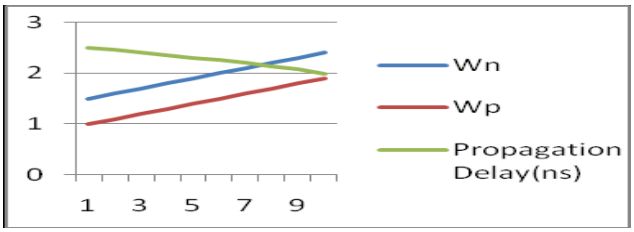
IV. RELATED WORKS

A. Propagation Delay

$$\tau_{PHL}=\frac{C_{load}}{k_n\left(V_{DD}-V_{T,n}\right)}\left[\frac{2V_{T,n}}{V_{DD}-V_{T,n}}+ln\left(\frac{4\left(V_{DD}-V_{T,n}\right)}{V_{DD}}-1\right)\right] \quad ---(1)$$

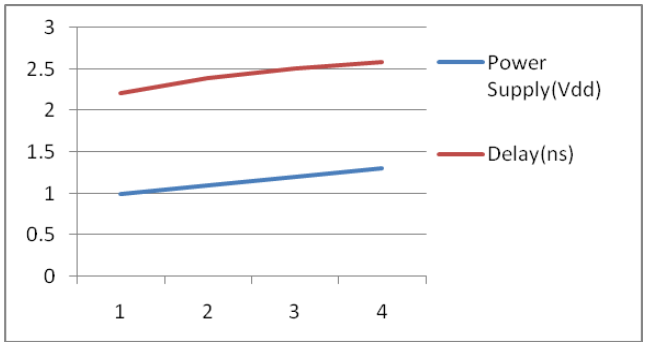
Where, $K_n = \mu_n C_{ox}(W/L)n$

In this paper we have already reduced channel length from 180nm to 90nm. From above equation (1) of propagation delay for cmos inverter, Graph 1. Shows that as well as we increase the width of transistor, the propagation delay decreases.



Graph 1.Variation of width with propagation delay

When we start to increasing the power supply V_{dd}, the propagation delay also increases. Due to need of less propagation delay we can't increase the power supply.



Graph 2.Variation of propagation delay with power supply

B. Power Consumption

Power consumption is very important factor for any circuit design

$$P_{avg} = \alpha C_L V_{DD}^2 f \text{ ------- (2)}$$

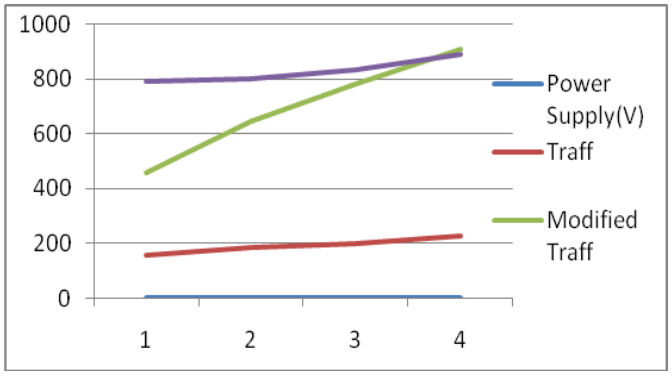
Where,

α- switching factor, C_L- Load Capacitance, V_{DD}- Power Supply, f- Switching frequency

In this paper we have reduced power supply from 1.8V to 1.2V, therefore all circuits have less power consumption. Equation (2) shows that if we increase power supply then power consumption also increases, at power supply of 1.2V an optimized result is achieved.

TABLE 1.VARIATION OF POWER CONSUMPTION WITH POWER SUPPLY

Power Supply(V)	Power Consumption(uW)		
	Traff	Modified Traff	FVF Based
1.5	226	908	890
1.4	201	782	832
1.3	184	641	798
1.2	**159**	**459**	**789**



Graph 3. Variation of Power Consumption with Power Supply

Graph 3 shows that relation between power consumption and power supply. Form this graph it is clear that if we increase power supply, power consumption is also increasing. To make better any circuit design it should have less power consumption. So in this paper we tried to get optimized result at power supply 1.2V.

V SIMULATION RESULTS

All the circuits have been simulated using Tanner Tool for 90nm CMOS technology. An input current of 50µA is used for all simulations. Fig. 6 shows the output waveform for the current comparator proposed by Traff at power supply of 1.2V. At this voltage, the output swing obtained is nearly 0.734V.

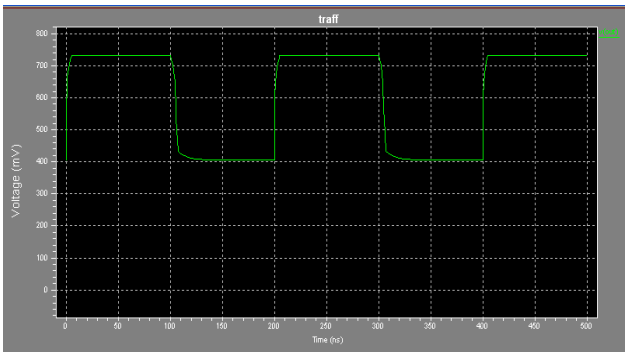


Fig. 6 Output waveform of Traff Current Comparator

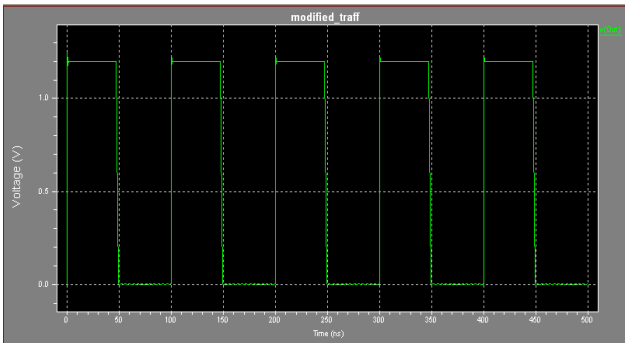


Fig. 7 Output waveform of Modified based Current Comparator

Fig. 7. Shows the output waveform of modified current comparator, for this circuit Output swing of 1.2V is obtained with a propagation delay of 1.74ns. Owing to the inverter stages added in order to achieve higher output

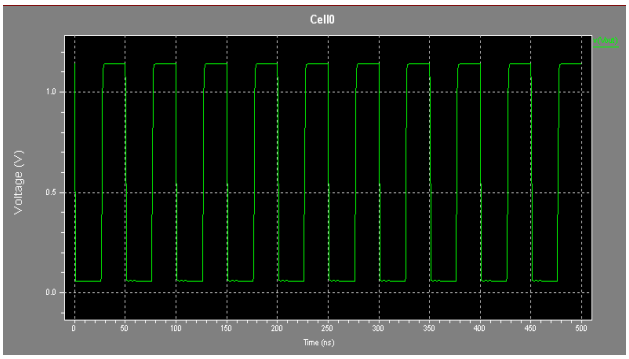


Fig. 8 Output waveform of FVF based Current Comparator

Fig. 8 shows the simulation results of the FVF based current comparator circuit at 1.2V power supply, for this circuit output voltage swing of 1.2V is obtained with a propagation delay of 0.227 ns. This structure employs only one additional CMOS inverter stage leading to a low transistor count as opposed to the modified Traff current comparator [1], which requires four stages.

TABLE II. PREVIOUS PAPER COMPARISION RESULTS [1]

Current Comparator	Traff	Modified Traff	FVF Based
Transistor Count	4	12	6
Propagation delay(ns)	9	1	0.75
Power Supply(V)	5	1.8	1.8
Output Swing(V)	0.725	1.8	1.8
Area Product	36	12	4.5

TABLE III. OUR APPROACH

Current Comparator	Traff	Modified Traff	FVF Based
Transistor Count	4	12	6
Propagation delay(ns)	2.54	1.74	0.227
Power Supply(V)	1.2	1.2	1.2
Output Swing(V)	0.734	1.2	1.1
Area Product	9.8	20.88	1.36

VI. CONCLUSIONS

An improved current comparator using FVF with voltage output is presented, which exhibits propagation delay of 0.227 ns and a relatively small area product. A comparison of the performance with different current comparators used has also been drawn at 1.2V power supply.

It can be observed from the above TABLE III that FVF based current comparator gives almost complete output voltage swing of 1.1V compared to 0.734V swing given by the compared structure. The delay decreases to 0.227ns. The area product of the FVF based configuration is very small as compare to modified Traff current comparator circuit.

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